ERROR CORRECTION FOR SYSTEM INTERCONNECTS

Abstract of the Disclosure

A system for error detection and correction in an interface between two portions of a data processing system is disclosed. The system includes a parity generator in a first portion of the data processing system. The parity generator generates parity bits corresponding to substantially the entirety of bits contained in the interface. The data and parity bits are transmitted across the interface. The system also includes a parity check in a second portion of the data processing system, for checking that the parity bits correspond to the bits for which parity was encoded. An error correction circuit is also provided, in a second portion of the data processing system, for correcting errors in the bits for which parity was encoded. An indication is optionally provided to the data processing system of corrected errors.